SOC-E

WHITEPAPER

Window violation and jitter calculations using Time Aware Shaper in a TSN network.

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Abstract

This paper presents a TSN platform from SOC-E, to which an IEEE 802.1Qbv and IEEE 802.1AS-2020 test case from SOC-E's TSN test plan will be performed. It aims to prove the proper performance of Time Aware Shaper in a TSN network.

In this paper, the test procedure, configuration, test setup and results needed to validate the jitter and window violation in a TSN network are presented.

The DUTs used in this test are RELY-TSN12 and RELY-10TSN12 from RelyUm by SOC-E. Meanwhile, the test station used are Paragon-X from Calnex and Novus ONE PLUS from Keysight.

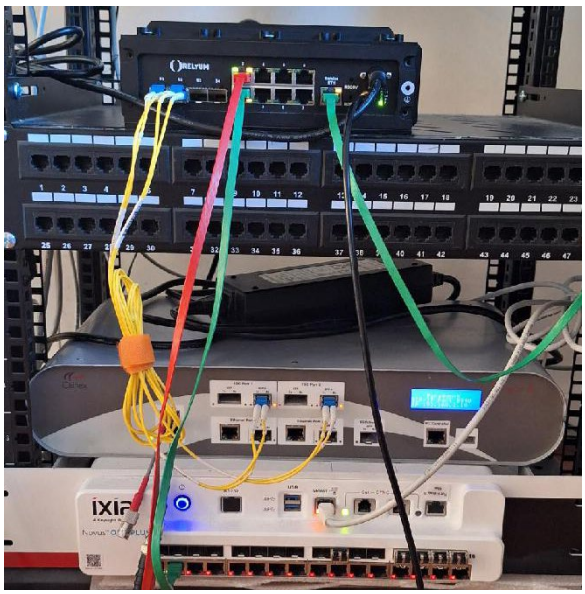


Figure 1: Test Setup

1. Introduction

Some applications and industries have a need of ensuring high priority frame delivery on specific time slots. Such applications usually transmit control data in controlled loop time and expect to receive the frames in their specific time slots with a known jitter and controlled latency. Time Aware Shaper (IEEE 802.1Qbv) ensures a controlled time delivery for those frames with time requirements.

The goal of this paper is to demonstrate the proper performance of the Time Aware Shaper, presented on chapter 2.1.

The obtained results are analyzed by a script which allows to determine if any window violation has happened and measures the jitter.

2. State of Art: Time-Sensitive Networking

Ethernet in Aerospace & Defense sector is increasingly becoming the main mode of communication between devices. Standard Ethernet, bus fields, synchronization mechanism and more recently Time Sensitive Networking (TSN) are used to ensure a proper communication.

TSN is emerging as a solution to ensure a deterministic Quality of Service (QoS) communication and unique solution based on Ethernet. The fundamental base of TSN is the mechanism named *Time Aware Shaper* (TAS), which its main goal is to separate the traffic in the network in fixed repetitive cycles (IEEE 802.1Qbv). These cycles can be divided into windows which can be assigned with one or more of the eight available priorities. On each window only the configured priorities will be forwarded.

To ensure the proper performance of TAS between all the nodes of the network a

synchronization protocol is used, IEEE 802.1AS-2020. This synchronization protocol ensures a nanosecond synchronization between the nodes that conform the network.

As TSN and all the mechanisms that conform TSN are relatively new, the required tests are yet to be developed. Organization such as Avnu and companies such as SOC-E, Keysight (Novus ONE PLUS) and Calnex (Paragon-X), among others, are developing test plans and test tools to prove the correct performance of the equipment, the proper work according to the defined standards and the interoperability between different equipment.

3. Platform (DUT)

Figure 2 shows the main architecture of SOC-E's TSN switch. The frames will arrive to the Rx interface port where they will be converted from electrical signals to digital signals by the PHY. These frames are then processed by the switch matrix engine that will forward them to the correct port according to the MAC table and the configured VLANs.

Then the "egress packet processing" module will determine, using IEEE 802.1Qbv, the correct order of the frames in the output buffer, so those frames are forwarded in the correct time slot.

The Tx port interface will forward the frames in the correct time slot as this module is synchronized to the 1588 timer (IEEE 802.1AS-2020).

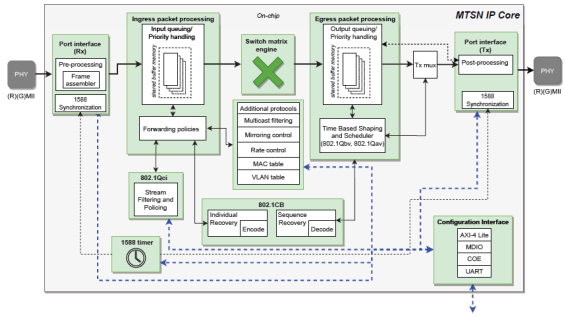


Figure 2-IP Core architecture

The SoC can be configured using an AMD Xilinx Ultrascale+ MPSoC system. The Processing System (PS) is constituted of a CPU that

processes the SW; this part is the fixed part of the integrate circuit. Meanwhile the Programable Logic (PL) refers to the FPGA, where the switching and TSN capabilities are implemented.

The PS system can configure the PL system using a custom Linux distribution developed by SOC-E, where all the necessary commands to configure the switching and TSN parameters are embedded. PS and PL system are communicated by an internal port by which the PL registers are configured. Figure 3 shows the architecture of the complete TSN switch RELY-TSN-BRIDGE+10TSN12.

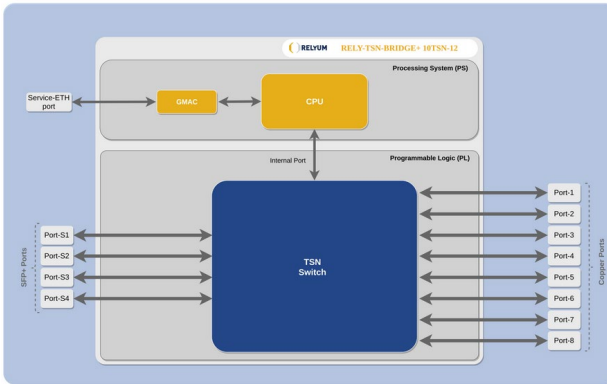


Figure 3: RELY-TSN12

For this test, a RELY-TSN12 (1Gbps speed) with a MTSN IP Core and a RELY-10TSN12 (10Gbps speed) with a TSN TGES IP Core will be used.

4. Test setup configuration

As explained in the previous chapter, the switch can be configured using different methods: CLI, Netconf or via web. In this case we will be using Netconf to configure IEEE 802.1Qbv and VLANs while AS will be configured using the web.

5. IEEE 802.1 AS-2020 configuration

The main goal of the test is to calculate the correct performance of IEEE 802.1Qbv, to check if it has any window violation and to measure the jitter of the first frame of each cycle time. As we are talking about nanoseconds measurements, a good synchronization between the DUT and the

test station is mandatory. To do so, IEEE 802.1AS-2020 must be correctly configured in the DUT. First of all, the Rx and Tx latencies of the ports must be calculated and validated.

To do so, Paragon-X test equipment will be used. Paragon-X can calculate values such correction field error, path turn delay and can also calculate the difference between the PPS provided by the DUT and the internal reference clock of Paragon-X.

So, using the path turn delay value provided by Paragon-X we can calculate the latencies of Rx and Tx using an iterative method where we change the configured latencies, and we look for the values of the PPS difference and the path turn delay to be as close as possible to 0ns.

With this correction we ensure a proper synchronization between DUT and test station.

Once the latencies are calculated and entered via web to the DUT, the DUT will be connected to Novus ONE PLUS test station. At Novus ONE PLUS, IEEE 802.1AS-2020 will be configured, where the first port will be configured as Master and the second one as

Slave. AS will be configured to send packets with priority 7 at the DUT.

6. IEEE 802.1Qbv configuration and VLANs

Netconf will be used to configure IEEE 802.1Qbv and VLANs in the DUT.

The test will be performed for three different speeds: 100M, 1G and 10G. The speeds of 100M and 1G will be performed in both RELY-TSN12 and RELY-10TSN12 and the speed of 10G will be executed only in RELY-10TSN12.

VLAN configuration is the same for all the speeds and for both equipment.

The traffic generated by the test station will be tagged with VLAN 2 and the DUT will be configured so PORT 1 and PORT 2 belong to VLAN 2. This will avoid any other traffic coming from the network to mess up with the test.

Port 1 and Port 2 from DUT will be configured as trunk in PVID 1, PCP 0, DEI 0, admitting all frames (tagged and untagged) and with egress tagging.

Also, a VLAN table entry will be created for VID 2. Port 1 and Port 2 will be added to this entry and removed from VLAN 1.

VID	VLAN Name	Egress port member	Untagged port members
1	Default VLAN	SWITCH/I,SWITCH/3-S4	SWITCH/I,SWITCH/3-S4
2	2	SWITCH/1-2	----

Table 1: VLAN configuration

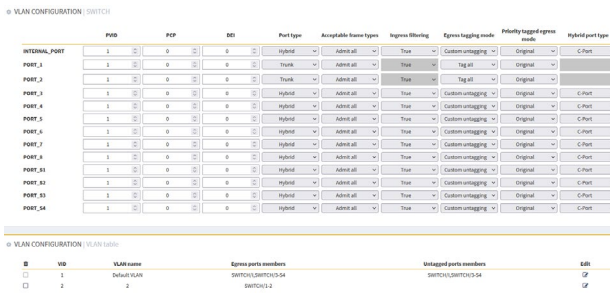


Figure 4: VLAN configuration

IEEE 802.1Qbv applies to the forward egress traffic, so in this case Port 2 will be configured. To configure IEEE 802.1Qbv, we must differentiate among the speeds.

The following table represents the configuration for IEEE 802.1Qbv for 1G in Port 2:

- Cycle time: 1000000ns
- Base time: 0s and 0ns

Time Slot	Time Interval(ns)	Q 0	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7
1	100000	O	X	X	X	X	X	X	X
2	25000	X	X	X	X	X	X	X	X
3	100000	X	O	X	X	X	X	X	X
4	25000	X	X	X	X	X	X	X	X
5	100000	X	X	O	X	X	X	X	X
6	25000	X	X	X	X	X	X	X	X
7	100000	X	X	X	O	X	X	X	X
8	25000	X	X	X	X	X	X	X	X
9	100000	X	X	X	X	O	X	X	X
10	25000	X	X	X	X	X	X	X	X
11	100000	X	X	X	X	X	O	X	X
12	25000	X	X	X	X	X	X	X	X
13	100000	X	X	X	X	X	X	O	X
14	25000	X	X	X	X	X	X	X	X
15	100000	X	X	X	X	X	X	X	O
16	25000	X	X	X	X	X	X	X	X

Table 2: IEEE 802.1-Qbv configuration

The configuration will open every cycle a time slot for each queue. To make sure no traffic exceeds its slot, a buffer time interval has been configured. During this time, no traffic should be forwarded.

For 100M the following differences of the configuration apply:

- Cycle time: 10000000ns
- Base time: 0s and 0ns
- Time intervals changes from 100000ns to 1000000ns and from 25000ns to 250000ns

For 10G the following differences of the configuration apply:

- Cycle time: 100000ns
- Base time: 0s and 0ns
- Time intervals changes from 100000ns to 10000ns and from 25000ns to 2500ns

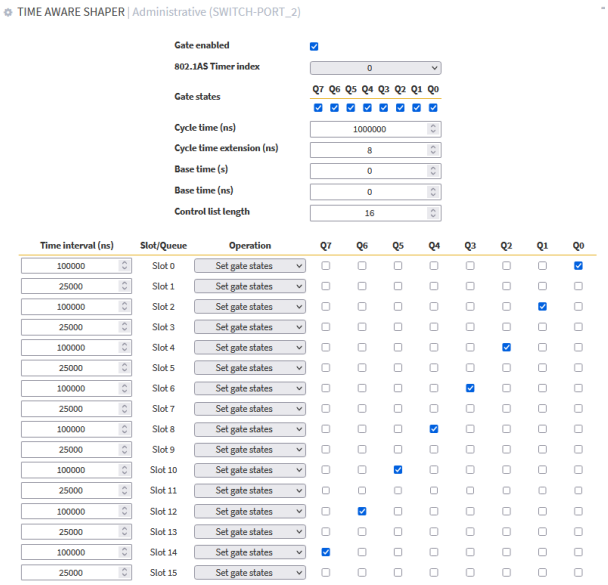


Figure 5: IEEE 802.1Qbv configuration for 1G

7. Test station (Novus ONE PLUS) configuration

As explained before, is mandatory for reliable results to have the test station correctly configured.

For this test, 2 topologies must be created in Novus ONE PLUS, both with Ethernet and PTP (IEEE 802.1AS-2020) capabilities.

Figure 6: Novus ONE PLUS topologies

Once the topologies have been created, IEEE 802.1AS-2020 must be configured, where topology 1 will work as Master and topology 2 as Slave with the following configuration:

- Delay Mechanism: P2P
- Multicast
- Domain 0
- Priority 1: 128
- Clock class: 6

Once IEEE 802.1AS-2020 is configured, it's time to configure the traffic. Eight traffics will be configured each one with a different priority.

Tx port	Rx Port	VLAN	Prior	Size	Rate	Bytes	(fr/s)
Port 1	Port 2	2	0	200	*(1)
Port 1	Port 2	2	1	200	*(1)
Port 1	Port 2	2	2	200	*(1)
Port 1	Port 2	2	3	200	*(1)
Port 1	Port 2	2	4	200	*(1)
Port 1	Port 2	2	5	200	*(1)
Port 1	Port 2	2	6	200	*(1)
Port 1	Port 2	2	7	200	*(1)

Table 3: Novus ONE PLUS traffic configuration

*(1) The rate has been calculated in chapter 5.1.

8. Test setup and connections

For this test two different setups must be made.

First the DUT must be connected to Paragon-X to calculate the correct latencies, Port 1 of DUT must be connected to Port 1 of Paragon-X and the PPS output of the DUT must be connected to Paragon-X PPS input.

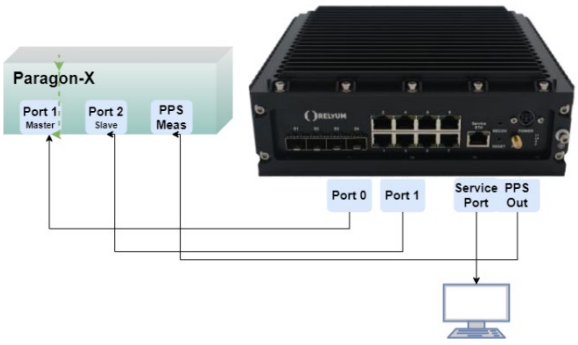


Figure 7: Paragon-X test setup

For the IEEE 802.1Qbv test, the following setup must be mounted with Keysight Novus ONE PLUS.

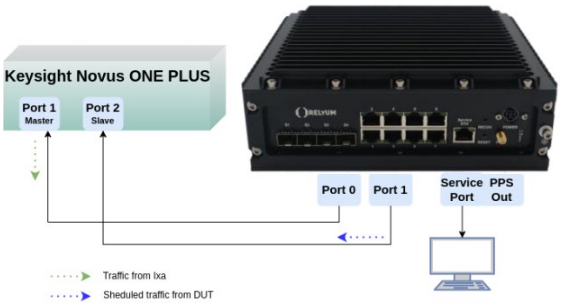


Figure 8: IEEE 802.1Qbv Novus ONE PLUS test setup

9. Results

9.1 Expected results

IEEE 802.1AS-2020 must have a proper synchronization to be able to calculate the jitter for IEEE 802.1Qbv. So, the offset between test station (Novus ONE PLUS) and the DUT must be less than:

Speed	Offset (ns)
1G	100
10G	50
100M	500

Table 4: Expected results for PPS error

This offset can be checked with Novus ONE PLUS's calculated statistics.

As per the expected results IEEE 802.1Qbv, we need to calculate the time it takes to send a packet:

$$Ts = (FrameSize + Preamble + IFG) * ByteSend\ Time + SwitchCycleTime$$

Frame size sent by Novus ONE PLUS is 200bytes, the preamble and the IFG together sum 20 bytes. The byte send time is 0,8ns for 10G, 8ns for 1G and 80ns for 100M.The SwitchCycleTime for a TGES is 6,4ns.

Knowing the time interval and the Ts we can get the frame rate:

$$FrameRate = \frac{TimeInterval}{\text{Ts}} * \frac{1000000000ns}{\text{CycleTime}}$$

Speed	Time Interval(ns)	Ts (ns)	Cycle time(ns)	Frame rate(ns)
1G	100000	1766.4	1000000	56612
10G	10000	182.4	100000	548245
100M	1000000	17606.4	10000000	5679

Table 5: Frame rate calculation

No frame should be lost with this configuration and an approximate of 80% of the line rate is achieved.

The distribution of the frames should be according to the opening slot of the IEEE

802.1Qbv configuration. To check that no frame has been forwarded out of its own time slot, the timestamping functionality of Novus ONE PLUS is used.

Novus ONE PLUS is capable of adding a timestamp to each packet with nanosecond precision. This timestamp is added both the moment the frame leaves the test station and the moment the frame arrives to the test station. As the test station is synchronized with the DUT, the timestamp on the arrival frame to the test station can be used to check if there has been any window violation and to calculate the jitter as shown in Figure 9.

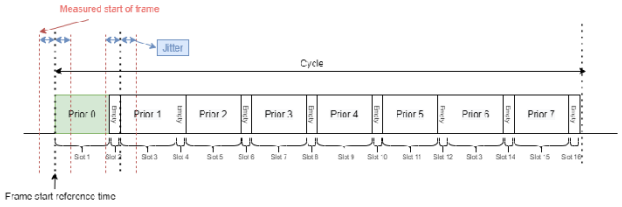


Figure 9: Jitter measurement

9.2 Obtained results.

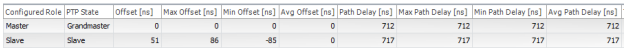
As explained in the previous chapter, first thing to consider must be a correct synchronization between DUT and Test Station, both Novus ONE PLUS and Calnex.

Calnex has been used to calculate the error in the synchronization.

Speed	Measured mean offset (ns)	Min (ns)	Max (ns)	Max-min	Std. Dev (ns)
1G	20.225	8	29	21	4.031
10G	-1.94	-11	8	19	3.202
100M	258.568	5	429	424	123.104

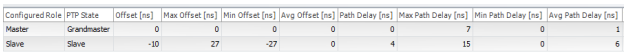
Table 6: IEEE 802.1AS-2020 results

Also, Novus ONE PLUS have been used to check that the synchronization is consistent.



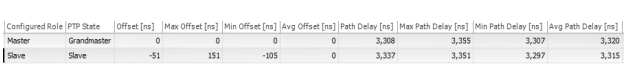
Configured Role	PTP State	Offset [ns]	Max Offset [ns]	Min Offset [ns]	Avg Offset [ns]	Path Delay [ns]	Max Path Delay [ns]	Min Path Delay [ns]	Avg Path Delay [ns]
Master	Grandmaster	0	0	0	0	712	712	712	712
Slave	Slave	51	86	-85	0	717	717	717	717

Figure 10-IEEE 802.1AS-2020 results Novus ONE PLUS 1G



Configured Role	PTP State	Offset [ns]	Max Offset [ns]	Min Offset [ns]	Avg Offset [ns]	Path Delay [ns]	Max Path Delay [ns]	Min Path Delay [ns]	Avg Path Delay [ns]
Master	Grandmaster	0	0	0	0	0	7	0	1
Slave	Slave	-10	27	-27	0	4	15	0	6

Figure 11: IEEE 802.1AS-2020 results Novus ONE PLUS 10G



Configured Role	PTP State	Offset [ns]	Max Offset [ns]	Min Offset [ns]	Avg Offset [ns]	Path Delay [ns]	Max Path Delay [ns]	Min Path Delay [ns]	Avg Path Delay [ns]
Master	Grandmaster	0	0	0	0	3,308	3,355	3,307	3,320
Slave	Slave	-51	151	-105	0	3,337	3,351	3,297	3,315

Figure 12: IEEE 802.1AS-2020 results Novus ONE PLUS 100M

And from the DUT's web it can be check that the synchronization is correct, that the ports have the correct role, and that the DUT identifies the test station as grand master (GM).

```
unibase-1.1.4-opensrc
INF:cbase:cb_ipcsocket_init:combase-1.1.3-opensrc
------------------------------------------------------------------------------
------------------------- GM synchronization status --------------------------
------------------------------------------------------------------------------

Domain number = 0
Current PTP instance clock ID = 70:F8:E7:D0:2A:A7:00:00
GM clock ID = 00:11:01:FF:FE:00:00:01
GM present = True
GM offset = 35 ns, GM rate ratio = 1.000036793

------------------------------------------------------------------------------
------------------------------ Port status -----------------------------------
------------------------------------------------------------------------------

Port name = PORT_1, Port oper = False, asCapable = False, Port state = Disabled

Port name = PORT_2, Port oper = False, asCapable = False, Port state = Disabled

Port name = PORT_3, Port oper = True, asCapable = False, Port state = Disabled

Port name = PORT_4, Port oper = True, asCapable = False, Port state = Disabled

Port name = PORT_5, Port oper = True, asCapable = False, Port state = Disabled

Port name = PORT_6, Port oper = True, asCapable = False, Port state = Disabled

Port name = PORT_7, Port oper = True, asCapable = False, Port state = Disabled

Port name = PORT_8, Port oper = True, asCapable = False, Port state = Disabled

Port name = PORT_S1, Port oper = True, asCapable = True, Port state = Slave
Path delay = 2 ns, NRR = 1.000036793

Port name = PORT_S2, Port oper = True, asCapable = True, Port state = Master
Path delay = 6 ns, NRR = 1.000036801

Port name = PORT_S3, Port oper = False, asCapable = False, Port state = Disable

Port name = PORT_S4, Port oper = False, asCapable = False, Port state = Disable
```

Figure 13: IEEE 802.1AS-2020 results DUT web

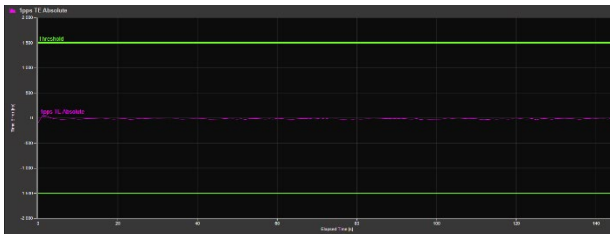


Figure 14: PPS 1G (Graphic)

Time Error 1pps TE	PASS
1pps TE Absolute Avg Time Error (cTE)	
Metric Statistics	
Mean [ns]	-19.103
Min [ns]	-102
Max [ns]	40
Max-Min [ns]	142
Std. Dev. [ns]	11.443

Figure 15: PPS 1G (Data)

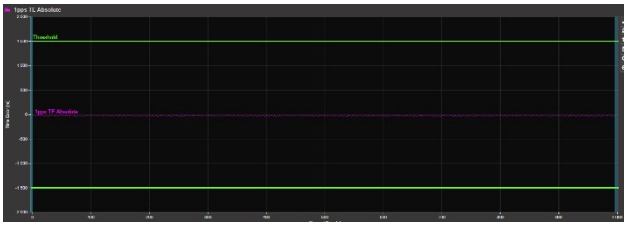


Figure 16: PPS 10G (Graphic)

Time Error 1pps TE	PASS
1pps TE Absolute Avg Time Error (cTE)	
Metric Statistics	
Mean [ns]	-29.947
Min [ns]	-41
Max [ns]	-20
Max-Min [ns]	21
Std. Dev. [ns]	3.486

Figure 17: PPS 10G (Data)

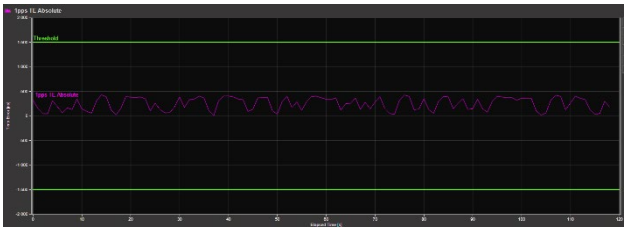


Figure 18: PPS 100M (Graphic)

Time Error 1pps TE	PASS
1pps TE Absolute Avg Time Error (cTE)	
Metric Statistics	
Mean [ns]	248.576
Min [ns]	5
Max [ns]	429
Max-Min [ns]	424
Std. Dev. [ns]	131.035

Figure 19: PPS 100M (Graphic)

Once a proper synchronization has been achieved, it is time to review the IEEE 802.1Qbv results.

AS explained in chapter 5.1 the main goal of the test is to check whether any window violation has happened. To check so, a python script has been developed. The Novus ONE PLUS test station marks every single frame in Rx with a timestamp that is recorded. As this timestamp

has been synchronized with the DUT, the frames should arrive at each time slot. So, each timestamp is checked to a nanosecond level to ensure that they are arriving at its correct time slot.

Figure 20, Figure 21 and Figure 22 shows that there is no window violation at all, by plotting the frame arrival distribution in a cycle time. In those images, all frames recorded are plotted as dots.

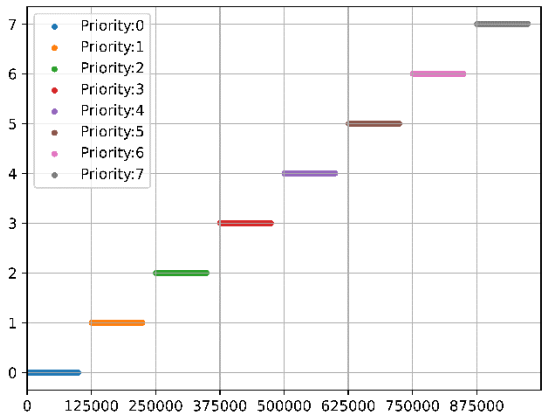


Figure 20: Frame window violation 1G

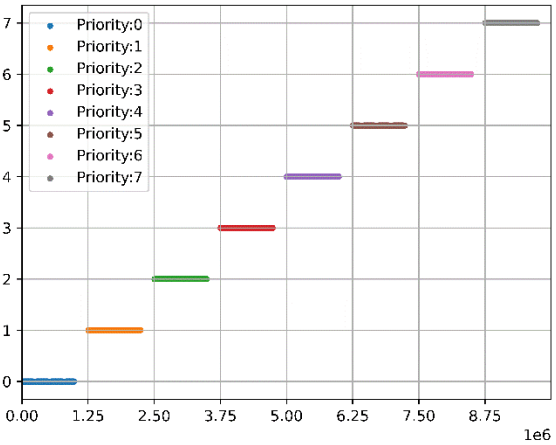


Figure 21: Frame window violation 10G

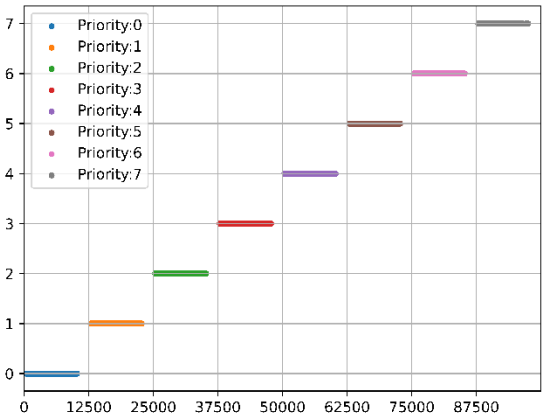


Figure 22: Frame window violation 100M

The image shows that every single frame arrives at their configured time slot. Also, it can be seen that between every time slot there is a buffer zone where no frame arrives.

The jitter is calculated considering the first frame of each priority that arrives every cycle time. With this information, we get the following results:

Speed	Priority	Mean jitter(ns)	Max jitter(ns)	Max jitter(ns)
1G	0	700.17	756	643
1G	1	700.29	756	651
1G	2	700.22	746	651
1G	3	700.19	746	643
1G	4	700.21	756	643
1G	5	700.27	756	651
1G	6	700.22	746	651
1G	7	700.45	1378	643
10G	0	412.77	1255	363
10G	1	412.49	450	368
10G	2	412.57	450	362
10G	3	412.63	453	365
10G	4	412.53	450	370
10G	5	412.61	450	365
10G	6	412.59	450	365
10G	7	412.58	450	368
100M	0	3754.63	3909.6	3666
100M	1	3754.63	3909.6	3666
100M	2	3754.14	3909.6	3666
100M	3	3754.46	3909.6	3666
100M	4	3754.17	3909.6	3666
100M	5	3754.79	3909.6	3666
100M	6	3754.46	3909.6	3666
100M	7	3772.55	20066	3666

Table 7:IEEE 802.1Qbv results

The calculated latencies by Novus ONE PLUS for each priority traffic are as they follow:

Speed	Priority	Store-forward Avg latency (ns)	Store-forward Min latency (ns)	Store-forward Max latency (ns)
1G	0	454943	4400	906195
1G	1	454943	4400	906195
1G	2	454940	4400	906195
1G	3	454942	4400	906185
1G	4	454943	4400	906195
1G	5	454945	4400	906185
1G	6	454944	4400	906195
1G	7	455458	4400	937272
10G	0	44525	0	89787
10G	1	44525	0	89790
10G	2	44522	0	89787
10G	3	44522	0	89787
10G	4	44525	0	89790
10G	5	44525	0	89790
10G	6	44522	0	89787
10G	7	44522	0	89787
100M	0	4516519	9930	9027370
100M	1	4516223	9930	9026890
100M	2	4516069	9930	9026650
100M	3	4516008	9930	9026730
100M	4	4515747	9930	9026490
100M	5	4516141	9930	9027530
100M	6	4516890	9930	9027530
100M	7	4673697	9930	9670170

Table 8-Latencies results

As part of the test and to check the importance of IEEE 802.1AS-2020 when using IEEE 802.1Qbv, a test with a 100% of frame rate has been made so IEEE 802.1AS-2020 cannot synchronize. It can be seen in Figure 23 that due to the lack of synchronization the frames arrive to the test station when they shouldn't, causing some window violations.

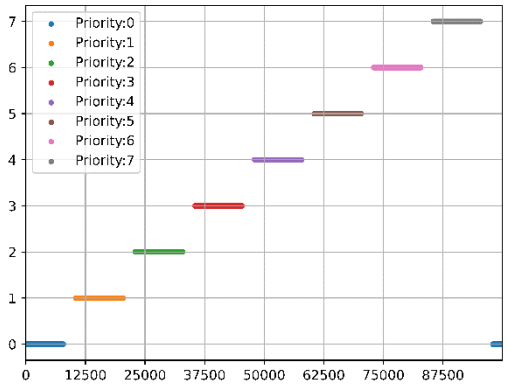


Figure 23: Bad AS synchronization

10. Conclusion and future work

This test shows the TSN capabilities of RELY-10TSN12 and RELY-TSN12 and the importance of a correct configuration of TSN.

During the it has been checked that IEEE 802.1AS-2020 and IEEE 802.1Qbv work properly, without any window violation and keeping a steady jitter in all frames. Also, a demonstration of how important a proper synchronization is, has been made.

This test is part of bigger TSN test plan that involves further testing for IEEE 802.1AS-2020 and IEEE 802.1Qbv.

Referencias

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